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Pre-Computation Based Self-Controlled Precharge-Free Content-Addressable Memory in High Speed Applications

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Abstract: Content-Addressable Memory (CAM) is frequently used in applications, such as lookup tables, databases, associative computing, and networking, that require high-speed searches due to its ability to improve application performance by using parallel comparison to reduce search time. Although the use of parallel comparison results in reduced search time, it also significantly increases power consumption. Both low power NAND-type and high-speed NOR-type match-line (ML) schemes suffer from requirement of the precharge prior to the search. Recently, a precharge-free ML structure has been proposed but with inadequate search performance. In this brief, a Pre-computation Based Self-Controlled Precharge-Free CAM (PB-SCPF CAM) structure is proposed for high-speed applications. The SCPF architecture is useful in applications where search time is very crucial to design larger word lengths. The experimental results show that PB-SCPF approach can achieve on average 80% in delay reduction and 32% in power reduction. The major contribution of this paper is that it presents theoretical and practical proofs to verify that our proposed PB-SCPF CAM system can achieve greater power reduction without the need for a special CAM cell design. This implies that our approach is more flexible and adaptive for general designs.

Keywords: Content-Addressable Memory (CAM), ML delay, high speed search, Self-Controlled Precharge-Free CAM.

I.INTRODUCTION

The persistence of present and future Internet usage mainly depends on performance and security issues. Content-addressable memory (CAM) is useful for high-performance forwarding, which performs the search in a single clock cycle [2], [3]. In a CAM, the user supplies the content to be searched, and the CAM gives back the address location or performs association. CAMs are used in numerous routing applications and hardwares such as network router, cache memories, longest prefix matching, and radix trees [4]–[6]. Therefore, many of the table lookup tasks at different network layers that were originally implemented in software are replaced by hardware solutions such as CAMs to meet the performance requirements.CAM stores the data in its memory through bit line drivers. The input data driver feeds the search content to CAM, which performs the search operation. There is a ML (Match Line) corresponding to each word, feeding into ML sense amplifiers (MLSAs), and there is a differential search line pair corresponding to each bit of the search word. A CAM search operation begins with loading the search-data word into the search-data registers followed by precharging all MLs high, putting them all temporarily in the match state. Next, the search line drivers broadcast the search word onto the differential search lines, and each CAM core cell compares its stored bit against the bit on its corresponding search lines. MLs on which all bits match remain in the precharged-high state. MLs that have at least one bit that misses, discharge to ground. The MLSA then detects whether its ML has a matching condition or miss condition. Finally, the encoder maps the ML of the matching location to its encoded address. The major challenges for CAM designers were to implement high-performance, low-power cells to meet the lower technology node requirements. Fig. 1 shows the conventional CAM organization, where the information is stored in rows and a parallel search is performed [6], [7]. CAM stores the data in its memory through bitline drivers. The input data driver feeds the search content to CAM, which performs the search operation. It produces the match address, if any stored data matches with the search content [7].

A sense amplifier is used to access the match information (hit/miss). Each search is performed followed by a precharge phase, a constraint to the faster search frequency. Designing a high-speed CAM for larger word lengths is a challenging task. Recently precharge-free CAM (PF-CAM) architectures have been presented [12]–[14], but these lack the search performance at higher word lengths. A self- controlled PF-CAM (SCPF-CAM) has been reported in this brief to avoid the dependence among CAM cells and to improve the frequency of operation.

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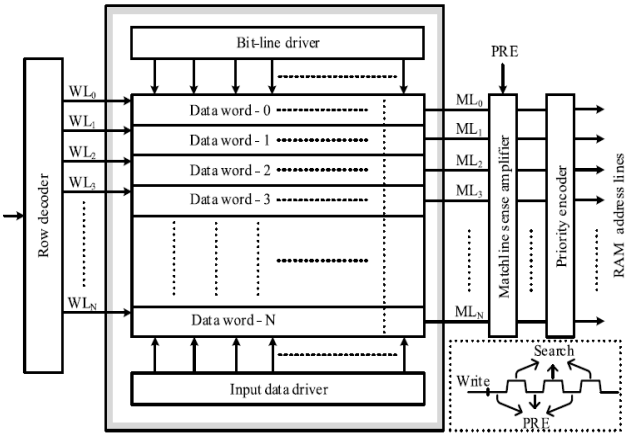

Fig. 1 Organization of a CAM Array and its Sensing Structure

The remainder of this brief is organized as follows: Section II describes the conventional NAND-type CAM operation. Section II describes the conventional NOR-type CAM operation. PF-CAMs are described in Section IV, where the proposed PB-SCPF CAM has been introduced. In Section V, the performance comparison results derived from the post layout simulations carried out on the compared designs of a 128 × 32-bit CAM array have been presented and Section VI concludes this brief.

II. NAND-TYPE CAM

NAND-type CAM cell is mainly used to reduce the power consumption of the system.In a conventional CAM, before performing a search, all match- lines (MLs) are to be precharged. This consumes more power as well as reduces the performance and frequency of operation due to requirement of an extra precharge phase. To eliminate unwanted frequent charging and discharging of all ML nodes, a precomputation stage is presented. In differential ML with a self-disabling sensing technique has been used to choke down the ML draining current. Employing differential ML instead of a single-ended ML helped boost the search speed without the overhead of power consumption. A search is performed in a CAM through three phases: data write, precharge, and data search.A NAND-type ML CAM cell, as shown in Figure consists of one SRAM cell and a pair of nMOS transistors in the comparison circuit and one nMOS transistor (M9) in evaluation logic. The bitline pair (BL, BL) has been used to store the data in the CAM cell and search-line pair (SL, SL) is used to search the content in CAM cell.

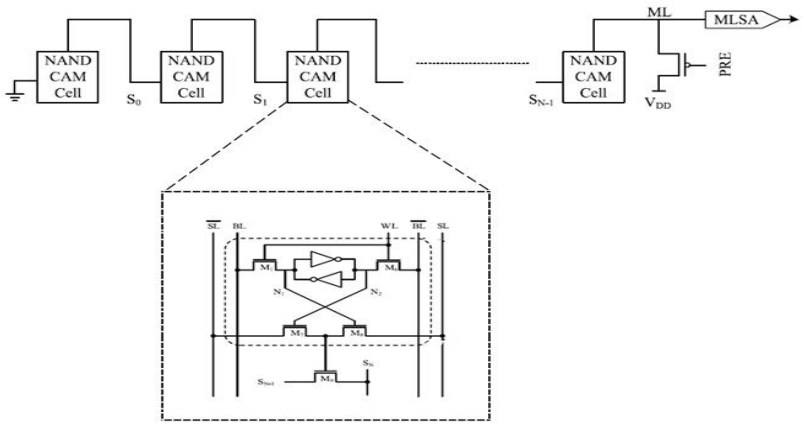

Fig. 2 Word Structure of NAND-Type CAM

Before performing a search, all MLs must be precharged to the supply voltage by keeping search-lines at low. If the search content matches with the stored data, ML discharges to a low value (GND); Otherwise ML remains at a precharged value. The ML has to be precharged before each search; therefore, NAND-type ML is not preferred for CAMs with long words because of the larger delay, and because it suffers from the charge-sharing problem across the PASS transistors. Due to this problem NAND-type ML is preferred only for CAM with a small word length.

Limitations of NAND-type CAM: ML (ML) has to be precharged before each search. The speed of search operation is limited by the precharge cycle. Due to its larger delay, speed of the search was reduced. It suffers from the charge-sharing problem across the pass transistors. NAND-type ML is preferred only for CAM with a small word length.

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III. NOR-TYPE CAM

NOR-type CAM cell is used for better performance of the system. And also improve the speed of the search operation.Conventional NOR CAM cell that consists of two parts: 1) one for storing data, called store unit; and 2) the other for comparing data, referred to as compare unit. The store unit is usually implemented as the traditional 8T SRAM cell that contains a cross coupled inverter pair. The compare unit is a pass-transistor logic (PTL) for comparing the stored with search data.

In NOR-type CAM design, the CAM cell is XOR-type, and the pull-down transistors of each CAM cell are arranged in NOR type. There are two phases in a search operation: Precharge phase and Evaluation phase. During the precharge phase, PRE = 1 will precharge the ML to high. Then, PRE is pulled down to 0 to start the evaluation phase. For a CAM word, if one or more cells are mismatched, the ML would be discharged to 0. Only when all cells are matched, i.e., the search data is identical to the stored data, the ML can retain logic high as in the precharge phase. Because the pull-down path is very short, in case of a mismatch the ML is discharged to 0 quickly. Thus, the NOR-type CAM provides the best search performance.

The pull-down transistors arranged in NOR type is beneficial for search performance, but they contribute a lot of drain capacitances to the ML. Because in many applications most of the CAM words are mismatched, a large number of ML switching would consume a huge dynamic power. For example, in the CAM tag used in the translation look-aside buffer or cache memory, at most one word is matched on each lookup, which implies that almost all the MLs would be discharged to 0, and then be charged to high before the next search. NOR-type CAM can provide the best performance.

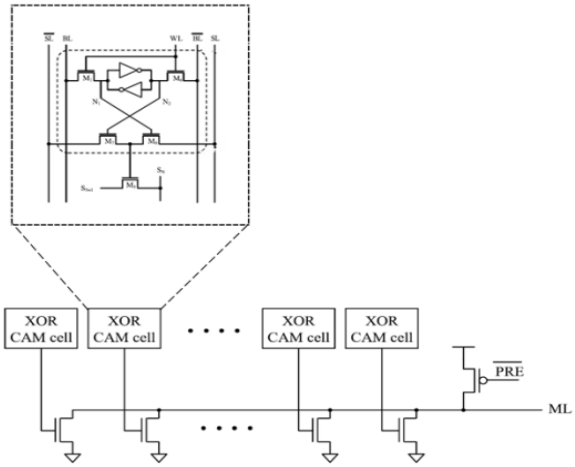

Fig. 3 Word Structure of NOR-Type CAM

In contrast to the NOR-type CAM, the NAND-type CAM aims to reduce the power dissipated in search operation, where the pull-down transistors of each CAM cell in the same word are arranged in NOR type. The ML is initially precharged to high, and discharged to 0 only when all CAM cells are matched. Because the load capacitance of ML is small and only a few MLs are discharged to 0 during a search, the power consumption is minimal. However, the pull-down path is too long, such that the ML discharge is very slow in case of a match.

Limitations of NOR-type CAM: NOR-type ML experiences SC current during the precharge phase. NOR-type CAM is power inefficient. It trades the poor performance for a large power saving. ML (ML) has to be precharged before each search.

IV. PRECHARGE-FREE ML STRUCTURE

A. Precharge-Free CAM

PF CAM is mainly proposed to perform the search operation for larger word lengths. Also improve the speed of the operation by remove the PRE phase.The development of a CAM structure is carried out with a PRE signal, which ends up at a lower speed of search operation.This drawback has been eliminated by removal of the PRE phase, as shown in Figure 3.3. Instead, they used control bits (CBs), which reduced the overall search time by one level. In a CAM, the first operation is write, followed by precharge, and then search. However, in the PF-CAM architecture, the write is followed directly by the search phases. The operation of the PF-CAM is as follows: 1) While storing the data, CB is set to a high value (logic 1). This setting of CB turns M0 OFF and, simultaneously, M1 ,……MN−1 will be turned OFF as T0 ,T1,……TN−1 are ON, which will provide GND directly to the gate of M1 ……MN−1, as shown in Figure 3.2)Once the data are stored, CB is reset (0) and this will turn ON M0 as M0 is a pMOS, since the source of M0 is connected as a control to M1 , thus S0 value is passed to the gate of M1 , which is an nMOS. If CAM cell-1 is matched, M0 will pass logic high to M1, which will result in turning ON of M1. If CAM cell-2 is also matched, then in a similar fashion logic high will be passed to M3 from CAM cell-2, and likewise a cascaded chain of CBs will

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be passed from one cell to another. If there is a mismatch at any cell, then the forthcoming cells will be turned OFF. Thus the PF-CAM structure gives advantage by reduction in the number of SC paths, which in turn results in overall reduction of power.Limitations of PF-CAM: Due to cascading of CAM cells overall, the speed of search operation is significantly reduced.

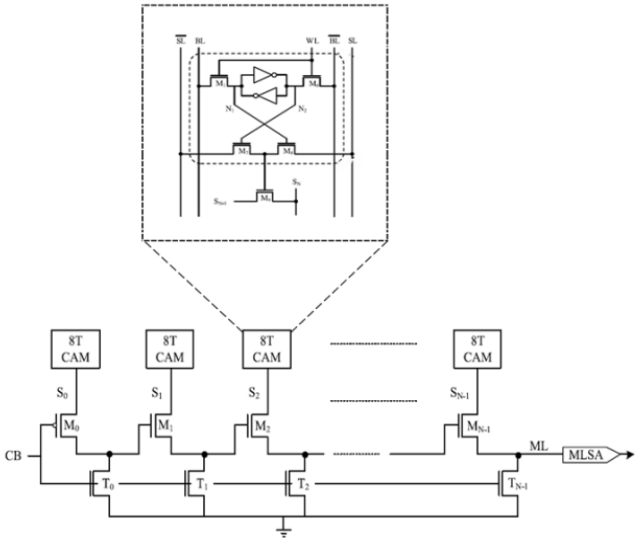

Fig. 4 Word Structure of PF CAM

B. Self-Controlled Precharge-Free CAM

SCPF-CAM structure, which solves the deficiency of all the mentioned problems present in the precharge-based CAMs and improves the speed of operation compared to the PF-CAM architecture. An 8T CAM cell has been used as the basic block to design a word. Two major contributions are made:

1) Self-control operation, where the charge stored at the node S controls the ML transistors, thereby avoiding the dependence on previous ML value.

2) The scheme eliminates the precharge phase to provide a higher search frequency.

The proposed PB-SCPF CAM is self-controlled; the node (S) value of the 8T CAM cell controls the evaluation logic and produces the output. If the search content matches the prestored data, then it pass a high value through the transistor (NMOS) .Otherwise it passes a low value through the transistor (PMOS) to the ML. From the word architecture, it is clear that the minimum operating voltage is limited to VTHP +2VTHN +VM. The voltage VM is mostly MLSA dependent and the most dominating among the three voltages.

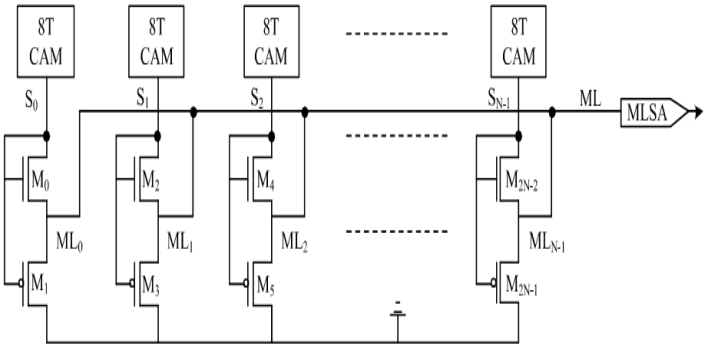

Fig. 5 Word Structure of SCPF-CAM

Transistor (NMOS) is chosen to have a low threshold to push the supply voltage scaling limit. A comprehensive comparison has been performed with NAND-CAM and PF-CAM for validating the efficiency of SCPF-CAM. The compared designs are analyzed at temperature variation and supply voltage scaling. Process variation is carried out explicitly to provide a better understanding of the device property and the application aspects of CAM.The minimum amount of time required in the conventional CAM operation is, Ttotal = Twrite + Tprecharge + Tsearch. However, in the proposed design the minimum requirement is, Ttotal = Twrite + Tsearch.

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C. Pre-computation Based Self-Controlled Precharge-Free CAM

In PB-SCPF CAM, the advantage of the SCPF-CAM structure is exploited; moreover, drawbacks of the precharge-based earlier reported circuits (which was cascading) are also taken care of by removing dependence among different CAM cells. The advantage of the proposed architecture is the design of larger word lengths with higher performance at a higher frequency of operation. Owing to the larger delay metric in PF-CAM, it is not useful for forming longer word lengths and cannot operate at a higher frequency of operation.

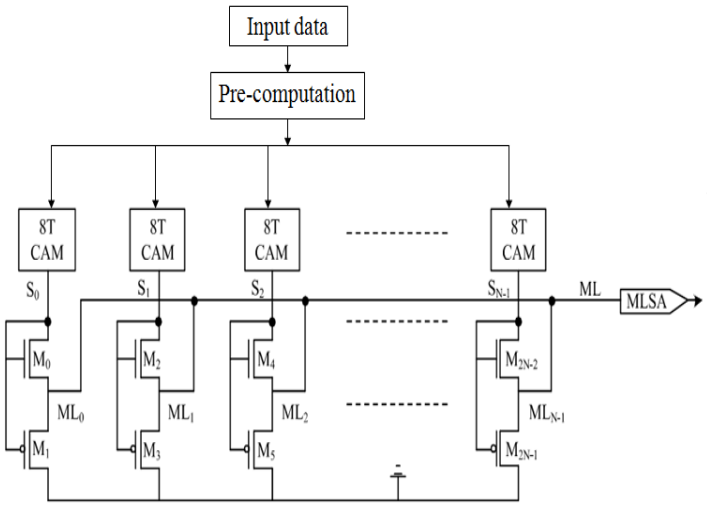

Fig. 6 Block Diagram of PB-SCPF CAM

In Precomputation Block, parity bit is introduced as parameter for comparison operations. The parity bit generator is a parameter extractor here that will be used for generating parity bit value. The advantage of using parity as a parameter is that parameter memory is highly reduced comparison with existing systems as only one bit i.e. k=1 is required for storing parameter corresponding to each stored word whatever may be the length of input data bits. Hence, the number of comparison operations in pre-computation is highly reduced and hence the power consumption of parameter memory. So, overall power consumption of the CAM is reduced. Compared with existing methods, the proposed architecture has improvement in complexity and area. The searching speed is also increased due to reduction in complexity and reduction in parameter comparison operations. By using parity bits, delay for each search operation is reduced. Hence, it boosts the search speed of parallel CAM.The number of bits having logic value '1' in a given binary data is counted. If number of bits in the binary data is odd, then the parity bit value is '1' and if the number of one's in a binary data is even, then the parity bit value is '0'. This process can be performed by using the circuit fig. 7.

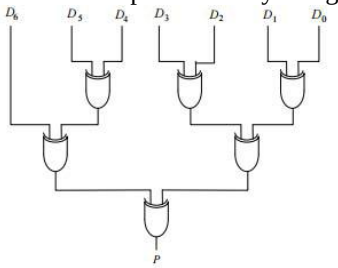

Fig. 7 Logic Circuit of Parity Bit Parameter Extractor

First the parity bit is extracted using parity bit generator and comparisons of extracted parity bit are made with that of stored parity bits. Then, according to the results of parity bit comparisons, a comparison in data memory takes place. Comparisons in data memory will be made only with those stored data words whose corresponding parity bit will be matched with that of input word's parity bit.

V. RESULT AND PERFORMANCE ANALYSIS

A. Design process

Tanner EDA provides a complete line of software solutions that catalyze innovation for the design, layout and verification of analog and mixed-signal integrated circuits. Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and Radio Frequency (RF) devices.

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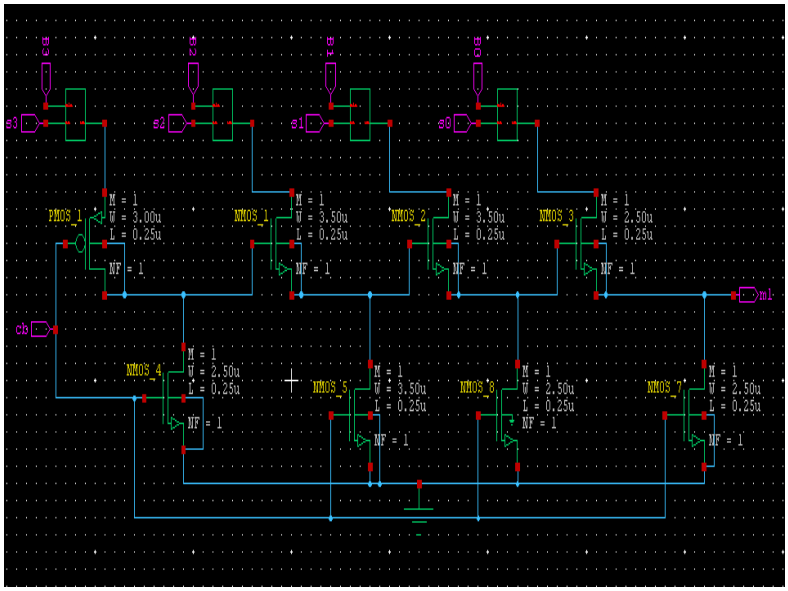

Fig. 8 Design of PF CAM

Fig. 8 shows the schematic diagram of single PF CAM design. From this design, 4*4 PF CAM was designed, which was shown in fig. 9. It draw in tanner EDA tool S-Edit window. Then it run by using T-spice. The output waveform shown in fig. 10 and their power analysis was done. The total power consumed is 0.00139 mW.

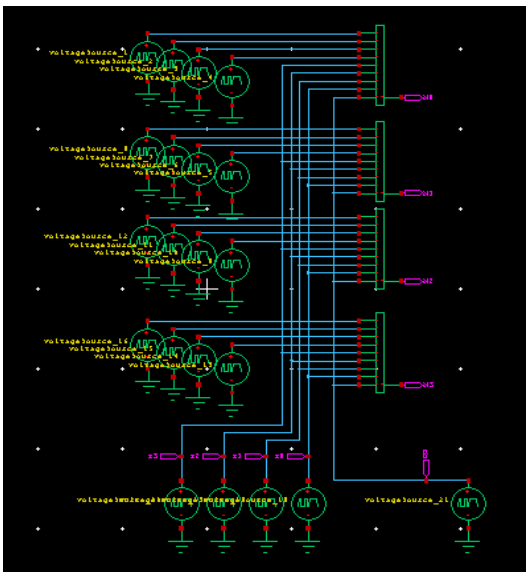

Fig. 9 Design of 4*4 PF CAM

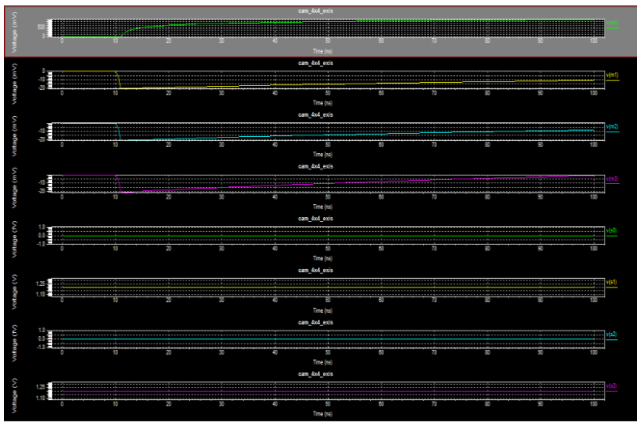

Fig. 10 Output Waveform of PF-CAM

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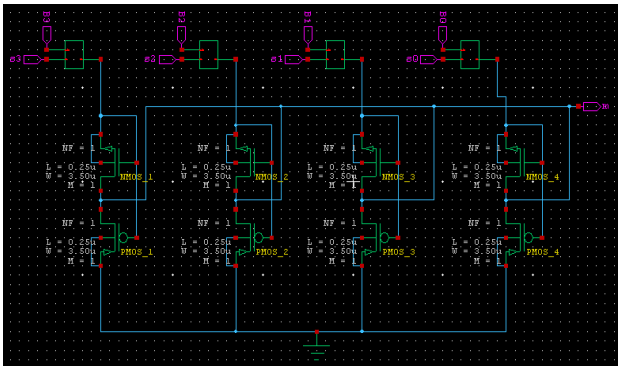

Fig. 11 Design of SCPF CAM

Fig. 11 shows the schematic diagram of single SCPF CAM design. From this design, 4*4 SCPF CAM was designed. It draw in tanner EDA tool S-Edit window. Then it run by using T-spice. The output waveform shown in fig. 12 and the power analysis was done. The total power consumed is 0.1338 mW.

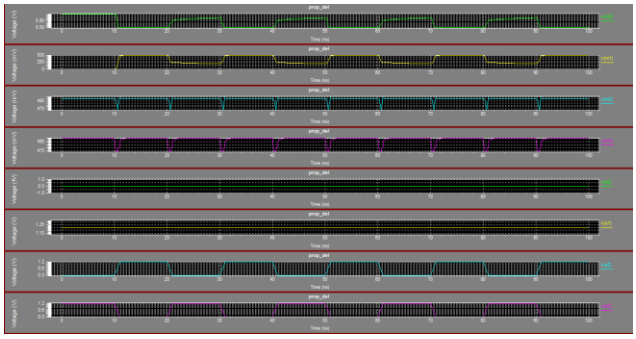

Fig. 12 Output Waveform of SCPF CAM

B. ML Delay Analysis

ML delay is considered a significant performance parameter in CAM design, and calculation and analysis are needed to measure the frequency of operation and its applicative aspects. An exhaustive analysis of ML delay was done on compared designs. Furthermore, its dependence on other parameters such as temperature and voltage has been accorded. It was observed that there was a gradual decre- ment in the delay metric as the temperature was increased; the related observations are depicted in Fig. 5(a). With increment in supply voltage, the delay also increases due to access time: the gate switching takes a longer time, since more charge has to be moved in an entire row and line delay is increased, as every wire has a capacitance. While increasing temperature, false match occurs in case of all the mismatched MLs in NAND-CAM. At above 40 °C temperature, the design does not work as the threshold drop decreases with the increase in temperature. There is a possibility of wrong state increases while increasing the temperature.

C. Process Variation Comparison

Process variation analysis is performed at different corners (FF, FS: Fast; SS, SF: Slow; TT: Typical) on the proposed and compared CAMs. The NAND-type ML CAM does not work at the extreme corners (FF and SS) after half the search time period; the mismatched ML values tend to match during the end of the search phase, which results in a wrong address output. The PF-CAM does not work at the slow corners due to VTH drop across the length of nMOS chain. For larger word length designs, the voltage at the final stage is less and is unable to drive the forthcoming cells due to the dependence between CAM cells. The SCPF-CAM works well at all these corners and the compared results are presented in Table II.

D. Search Delay Reduction by Proposed SCPF-CAM

Owing to the ability of the proposed design to operate without a PRE phase, there was a significant reduction in the delay (considering the PRE time), which yielded our design to work at a higher search frequency with respect to the compared designs. We achieved a 73% and 88% reduction in delay compared to NAND-CAM and PF-CAM, respectively, at 27 °C and VDD of 1 V. Due to this advantage in the ML delay reduction, more searches can be performed, which in turn will result in a reduction in the required number of search bits. This allows the design of larger word structures with higher performance; the related results are depicted in Fig. 5(b).

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E. Performance Comparison Summary

The performance summary of the compared designs is summarized in Table III. The SCPF-CAM produces ML value in the least time among the compared designs at the cost of minuscule additional dissipation. With increase in supply voltage, increment in peak power is observed in all the compared designs. The peak power comparison is illustrated in Fig. 5(c) at different temperatures. In PF-CAM, a significant growth in peak power is observed. This particular incre- ment is very less in our proposed design. The proposed SCPF-CAM consumes lesser peak power compared to other designs. A mismatch in a cell disables the charging of the ML segments present next to it. The NAND-type and PF-CAM are sensitive to the data pattern and process corner. The performance degrades for these designs at high ML-size and at low supply voltage. Transistor M9 in the SCPF-CAM cell presented in Fig. 2 has low voltage threshold, which is the reason for additional energy dissipation. The importance of it is described through the worst case scenario of the 1-bit mismatch summarized in Table IV at various search durations. The presented design performance is reasonable at this condition, but the other designs do not function. The proposed scheme performs well even at lower search durations, while the compared designs do not function at lower search durations. A comparison summary with the prior work is mentioned in Table V. The referred designs require a PRE phase, but in the proposed design this phase is eliminated and, thus, one phase delay is reduced. The ML delay is higher than in some of the compared designs, but the search does not take the PRE phase duration of T ns into account, and this increases the frequency of operation.

VI. CONCLUSION

An PB-SCPF CAM structure is proposed for high-speed applications, which exhibits the least ML delay among the compared designs. The proposed scheme avoids the PRE phase and nullifies the dependence between CAM cells in a word due to the self-control scheme. This gives an advantage to perform more searches within a stipulated time. The ML delay of the proposed scheme is 80% of PF-CAM, at the cost of trivial additional dissipation. This shall be of interest among designers for forming larger word lengths at better search speed.

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